Abstract of the Disclosure

A device and method for layout and fabrication of power supply bus lines in an integrated circuit such as a memory circuit are described. In accordance with the present invention, power bus lines and bonding pads of the circuit are not necessarily formed in both edge regions and center regions of the device. The bonding pads are formed in the region according to the package being used, and the power bus lines are formed in the other region. This is accomplished by forming the bonding pads over landing pads. Landing pads are formed in both the center region and the edge region under the top surface of the device. If the device is to be packaged in an edge pad configuration, the bonding pads are formed over the landing pads in the edge region, and power supply bus lines can be formed over the landing pads in the center region. Similarly, if the device is to be packaged in a center pad configuration, the bonding pads are formed over the landing pads in the center region, and the power supply bus lines can be formed over the landing pads in the edge region. The bonding pads are connected to the landing pads by conductive vias. Because the power bus lines are not formed in the same region as bonding pads, they can occupy a relatively large portion of the region in which they are formed. That is, they can be made much larger than they would be using the conventional approach in which both bonding pads and power bus lines are formed in the same region. As a result, the power noise drawbacks of the conventional approach are eliminated.

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